## Amendments To The Claims

The listing of claims presented below will replace all prior versions, and listings, of claims in the application.

**Listing of claims:**

1. (**currently amended**) A method for forming bit lines**, each bit line having a width,** of a semiconductor device, comprising the steps of:

forming a plurality of word lines and dopant areas on a semiconductor substrate;

forming a first inter-insulation layer on the substrate including the word lines, the first inter-insulation layer including landing plug contacts exposing a part of each dopant area;

forming landing plugs for embedding the landing plug contacts;

forming second and third inter-insulation layers in that order on a front surface of the substrate including the landing plugs;

**forming a fourth mask pattern by a Damacene process on the third inter-insulation layer, wherein the mask pattern defines etching areas at least substantially along the width of each to-be-formed bit line;**

forming bit line contacts for exposing the landing plugs by etching ~~of~~ the third and second inter-insulation layers **according to the fourth mask pattern, wherein each bit line contact is formed within the width of the bit line**; and

forming bit lines for embedding the bit line contacts.

2. (original) A method as claimed in claim 1, wherein the word lines each include a gate insulation layer, a gate electrode and a hard mask, the gate electrode having a structure of any one of a combination of polycrystalline silicon layer and a tungsten silicide layer, and a tungsten layer.

3. (**currently amended**) A method as claimed in claim 1, wherein the step of forming ~~**bit line contacts**~~ **a fourth mask pattern** comprises the sub-steps of:

**forming a fourth inter-insulation layer on the third inter-insulation layer;**

forming photosensitive layer pattern on the fourth inter-insulation layer, areas for the bit line contacts being defined on the photosensitive layer pattern;

forming ~~**a fourth inter-insulation layer**~~ **the fourth mask** pattern by etching ~~**of**~~ the fourth inter-insulation layer using the photosensitive layer pattern as a mask; **and**

removing the photosensitive layer pattern~~; and~~

~~**forming the bit line contacts for exposing the landing plug contacts by etching of the third and second inter-insulation layers using the fourth inter-insulation layer pattern as a mask**~~.

4. (**currently amended**) A method as claimed in claim 1 or 3, wherein the third inter-insulation layer makes use of any one of ~~**an**~~ **a** HTO (High Temperature Oxide) layer and a silicon-nitride layer, and the ~~**fourth**~~ **second** inter-insulation layer makes use of a material having an etching ratio different from that of the second inter-insulation layer.

5. (**currently amended**) A method as claimed in **claim 1** ~~claim 1 or 4~~, wherein the third inter-insulation layer is made of any one of BPSG (Boro-Phosphor-Silicate Glass) and TEOS (Tetra-Ethyl-Ortho-Silicate).

6. (**currently amended**) A method as claimed in claim 1, wherein the bit line contact holes are formed in a self-align contact mode**, wherein during an etching process, the etching area for each bit line contact is defined entirely within a bit line by the fourth mask pattern**.

7. (original) A method as claimed in claim 1, wherein the bit lines are of any one of a combination of polysilicon with tungsten-silicide, and a metallic substance.

8. (**new**) A method as claimed in **claim 4** ~~claim 1 or 4~~, wherein the third inter-insulation layer is made of any one of BPSG (Boro-Phosphor-Silicate Glass) and TEOS (Tetra-Ethyl-Ortho-Silicate).

**Amendments To The Drawings:**

The attached sheets of drawings include changes to FIG. 4D. This sheet contains corrections shown in red for the Examiner's approval and are requested to replace the original sheet of FIG. 4.

Attachment: Replacement Sheet of FIG. 4